NVT4555

SIM card interface level translator and supply voltage LDO

Rev. 2 — 24 May 2013 Product data sheet

1. General description

The NVT4555 device is built for interfacing a SIM card with a single low-voltage host side interface. The NVT4555 contains an LDO that can deliver two different voltages, 1.8 V or 2.95 V from typical mobile phone battery voltages up to 5.25 V and three level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller.

The NVT4555 contains one voltage select pin (CTRL) to select either 1.8 V or 2.95 V for SIM card power supply and one active HIGH enable pin (EN) to enable normal operation. The NVT4555 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

2. Features and benefits

- Support SIM card supply voltages 1.8 V and 2.95 V
- Input voltage range to LDO: 2.5 V to 5.25 V
- Host microcontroller operating voltage range: 1.1 V to 3.6 V
- Automatic level translation of I/O, RSTn and CLKn between SIM card and host side interface with capacitance isolation
- Low current shutdown (EN = 0) mode < 1 μA
- Supports clock speed beyond 5 MHz clock
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- ±8 kV IEC61000-4-2 ESD protected on all SIM card contact pins
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 12-pin WLCSP package (1.19 mm × 1.62 mm × 0.56 mm (nominal), 0.4 mm pitch)

3. Applications

- NVT4555 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4555UK	4555	WLCSP12	wafer level chip-size package; 12 bumps; body 1.19 × 1.62 × 0.56 mm	NVT4555UK

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NVT4555UK	NVT4555UKZ	WLCSP12	Reel 7” Q1/T1 *special mark chips DP	3000	T_{amb} = −40 °C to +85 °C

5. Functional diagram

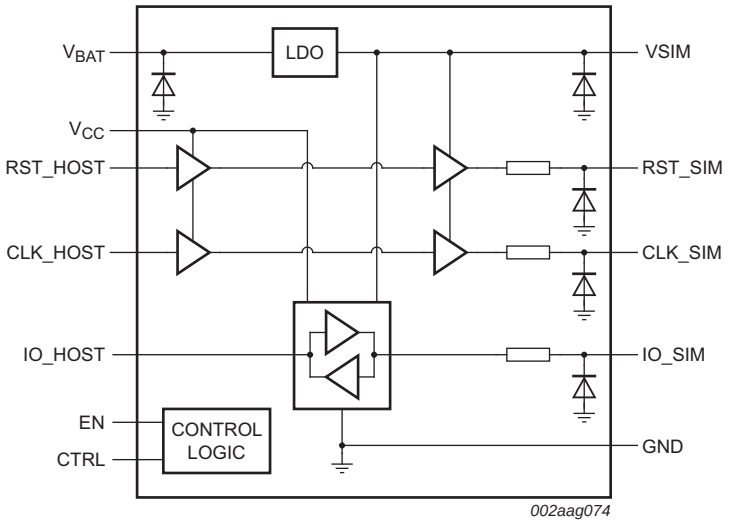

Fig 1. Functional diagram

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6. Pinning information

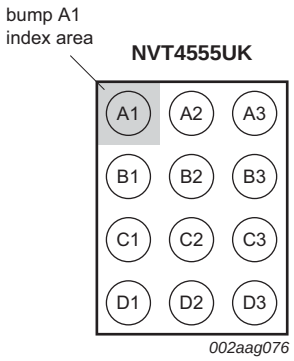

Fig 2. Bump configuration for WLCSP12

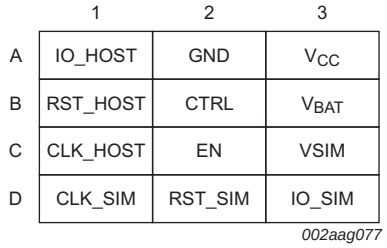

Fig 3. Bump mapping for WLCSP12

6.1 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
EN	C2	I	Host controller driven enable pin. This pin should be HIGH (V_{CC}) for normal operation, and LOW to activate a low current shutdown mode.
CTRL	B2	I	VSIM voltage select pin. A LOW level selects VSIM = 1.8 V, while driving this pin to V_{CC} selects VSIM = 2.95 V.
V_{CC}	A3	power	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). When V_{CC} is below the UVLO threshold, the VSIM supply is disabled. This pin should be bypassed with a 0.1 μF ceramic capacitor close to the pin.
V_{BAT}	B3	power	Battery voltage supply for internal LDO. This input voltage ranges from 2.5 V to 5.25 V. This pin should be bypassed with a 1.0 μF ceramic capacitor close to the pin.
VSIM	C3	power	SIM card supply voltage from internal LDO. The voltage at this pin can be selected for either 1.8 V (CTRL = 0) or 2.95 V (CTRL = 1). This pin should be bypassed with a 4.7 μF ceramic capacitor close to the pin.
IO_SIM	D3	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.
RST_SIM	D2	O	Reset output pin for the SIM card.
GND	A2	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
CLK_SIM	D1	O	Clock output pin for the SIM card.
CLK_HOST	C1	I	Clock input from host controller.
RST_HOST	B1	I	Reset input from host controller.
IO_HOST	A1	I/O	Host controller bidirectional data input/output. This output must be on an open-drain driver.

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7. Functional description

Refer to Figure 1 “Functional diagram”.

7.1 Function table

Table 4. Function selection

0 = GND; 1 = V_{CC}; X = don’t care.

CTRL input	EN input	VSIM output voltage
X	0	0 V
0	1	1.8 V
1	1	2.95 V

7.2 Shutdown sequence of NVT4555

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM, IO_SIM and VSIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before V_{BAT} and V_{CC} supplies go LOW to ensure that the shutdown sequence is properly initiated.

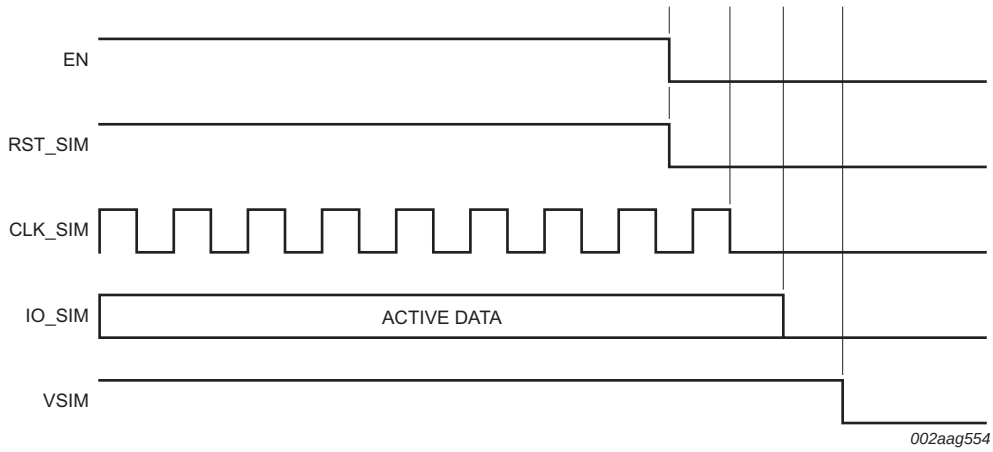

Fig 4. Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and VSIM of NVT4555 SIM card translator

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	SIM card side and VSIM pins; IEC 61000-4-2	[1]	-	±8	kV
		all other pins; IEC 61000-4-2	[1]	-	±2	kV
		all other pins; HBM	[2]	-	±2	kV
		all other pins; CDM	[3]	-	±500	V
V_{CC}	supply voltage			GND – 0.5	3.6	V
V_{BAT}	battery supply voltage			GND – 0.5	5.5	V
$V_{I(CLK_HOST)}$	input voltage on pin CLK_HOST	input signal voltage, HOST side		GND – 0.5	V_{CC} + 0.5	V
$V_{I(RST_HOST)}$	input voltage on pin RST_HOST	input signal voltage, HOST side		GND – 0.5	V_{CC} + 0.5	V
$V_{I(IO_HOST)}$	input voltage on pin IO_HOST	input signal voltage, HOST side		GND – 0.5	V_{CC} + 0.5	V
$V_{I(CLK_SIM)}$	input voltage on pin CLK_SIM	input signal voltage, SIM side		GND – 0.5	$V_{O(reg)}$ + 0.5	V
$V_{I(RST_SIM)}$	input voltage on pin RST_SIM	input signal voltage, SIM side		GND – 0.5	$V_{O(reg)}$ + 0.5	V
$V_{I(IO_SIM)}$	input voltage on pin IO_SIM	input signal voltage, SIM side		GND – 0.5	$V_{O(reg)}$ + 0.5	V
T_{stg}	storage temperature			–55	+125	°C
T_{amb}	ambient temperature			–40	+85	°C

[1] IEC 61000-4-2, level 4, contact discharge.

[2] Human Body Model (HBM) according to JESD22-A-A114.

[3] Charged-Device Model (CDM) according to JESD22-C101.

9. Characteristics

Table 6. Supplies

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.1 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{CC}	supply voltage		1.1	-	3.6	V
I_{CC}	supply current	operating mode; f_{clk} = 1 MHz	-	5	10	µA
		shutdown mode; EN = GND	-	-	1	µA
V_{BAT}	battery supply voltage		2.5	-	5.25	V
I_{BAT}	battery supply current	operating mode; IO_HOST = V_{CC}; CLK_HOST = RST_HOST = GND	-	20	30	µA
		shutdown mode; EN = GND	-	-	1	µA
$V_{th(UVLO)}$	undervoltage lockout threshold voltage	V_{CC} rising; V_{BAT} = 3.6 V	0.7	-	1	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage		-	100	-	mV

[1] Typical values measured at 25 °C.

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Table 7. Static characteristics

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.1 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	EN/CTRL pin threshold					
		1.8 V ≤ V_{CC} ≤ 3.6 V		0.7 × V_{CC}	-	V_{CC} + 0.2	V
		1.1 V ≤ V_{CC} < 1.8 V		0.85 × V_{CC}	-	V_{CC} + 0.2	V
V_{IL}	LOW-level input voltage	EN/CTRL pin threshold		−0.15	-	0.15 × V_{CC}	V
LDO							
$V_{O(reg)}$	regulator output voltage	VSIM pin; CTRL = EN = V_{CC}; 3.1 V ≤ V_{BAT} ≤ 5.25 V; 0 mA ≤ I_{SIM} ≤ 50 mA		2.85	2.95	3.1	V
		VSIM pin; CTRL = 0 V; EN = V_{CC}; 2.5 V ≤ V_{BAT} ≤ 5.25 V; 0 mA ≤ I_{SIM} ≤ 50 mA		1.7	1.8	1.9	V
V_{do}	dropout voltage	I_O = 50 mA; V_{BAT} = 2.90 V		-	100	150	mV
$I_{O(sc)}$	short-circuit output current	VSIM shorted to GND		90	135	170	mA
$t_{startup}$	start-up time	VSIM = 1.8 V or 2.95 V; I_O = 50 mA; C_o = 1 µF		-	-	400	µs
$T_{j(sd)}$	shutdown junction temperature			-	160	-	°C
$T_{sd(hys)}$	hysteresis of shutdown temperature			-	20	-	°K
R_{pd}	pull-down resistance	VSIM discharge; EN = GND; V_{BAT} = 3.6 V; V_{CC} = 1.2 V		-	100	-	Ω
PSRR	power supply rejection ratio	V_{BAT} = 3.6 V; I_{SIM} = 20 mA; VSIM = 1.8 V or 2.95 V					
		f = 1 kHz		-	60	-	dB
		f = 10 kHz		-	50	-	dB
Level shifter							
V_{IH}	HIGH-level input voltage	IO_HOST, RST_HOST, CLK_HOST					
		1.8 V ≤ V_{CC} < 3.6 V	[2]	0.7 × V_{CC}	-	V_{CC} + 0.2	V
		1.1 V ≤ V_{CC} < 1.8 V	[2]	0.85 × V_{CC}	-	V_{CC} + 0.2	V
		IO_SIM	[2]	0.7 × $V_{O(reg)}$	-	$V_{O(reg)}$ + 0.2	V
V_{IL}	LOW-level input voltage	IO_HOST, RST_HOST, CLK_HOST	[2]	−0.15	-	0.15 × V_{CC}	V
		IO_SIM	[2]	−0.15	-	0.15 × $V_{O(reg)}$	V
R_{PU}	pull-up resistance	IO_SIM connected to VSIM	[3]	4	6	8	kΩ
		IO_HOST connected to V_{CC}	[3]	3.5	5	6.5	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = −1 mA	[2]	-	0.7 × $V_{O(reg)}$	$V_{O(reg)}$	V
		IO_SIM; I_{OH} = −10 µA	[2]	-	0.7 × $V_{O(reg)}$	$V_{O(reg)}$	V
		IO_HOST; I_{OH} = −10 µA	[2]	-	0.7 × V_{CC}	V_{CC}	V

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Table 7. Static characteristics *...continued*

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.1 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA	[2]	-	100	300	mV
		IO_SIM; I_{OL} = 1 mA	[2]	-	100	300	mV
		IO_HOST; I_{OL} = 1 mA	[2]	-	100	300	mV
R_{pd}	pull-down resistance	CLK_HOST, RST_HOST; EN = 0		70	100	130	kΩ
EMI filter							
R_s	series resistance	IO_SIM	[2]	-	200	-	Ω
		RST_SIM		-	200	-	Ω
		CLK_SIM	[2]	-	200	-	Ω
C_{io}	input/output capacitance	IO_SIM	[2]	-	45	-	pF
		RST_SIM		-	45	-	pF
		CLK_SIM	[2]	-	45	-	pF

[1] Typical values measured at 25 °C.

[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.

[3] See Figure 8 for details.

Table 8. Dynamic characteristics

2.5 V ≤ V_{BAT} ≤ 5.5 V; f_{clk} = f_{io} = 1 MHz; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Refer to Figure 5.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC} = 1.8 V; CTRL = V_{CC} (VSIM = 2.95 V); SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side	[1]	-	8	15	ns
		all channels; host side to SIM card side	[1]	-	8	15	ns
t_t	transition time		[1]	-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[2]	-	2	-	ns
V_{CC} = 1.2 V; CTRL = V_{CC} (VSIM = 1.8 V); SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF							
t_{PD}	propagation delay	I/O channel; SIM card side to host side	[1]	-	15	25	ns
		all channels; host side to SIM card side	[1]	-	15	25	ns
t_t	transition time		[1]	-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM	[2]	-	2	-	ns
f_{clk}	clock frequency	CLK_SIM		-	-	5	MHz

[1] All dynamic measurements are done with a 50 pF load. Rise times are determined by internal pull-up resistors.

[2] Skew between any two outputs of the same package switching in the same direction with the same C_L.

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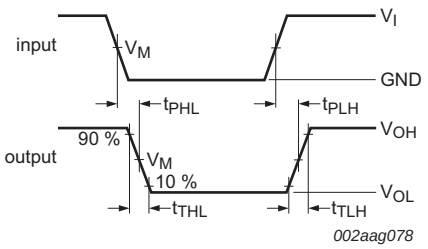
9.1 Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Data input to data output propagation delay times

10. Application information

The application circuit for the NVT4555, which shows the typical interface with a SIM card, is shown in Figure 6. The Low-DropOut (LDO) regulator, internal to the NVT4555, is designed to supply the SIM card power with a high Power Supply Rejection Ratio (PSRR) at a very low drop-out voltage ($V_{BAT} - V_{O(reg)}$). The LDO regulator provides two levels of fixed voltage regulation at 1.8 V or 2.95 V, which are selected with the CTRL pin of the NVT4555.

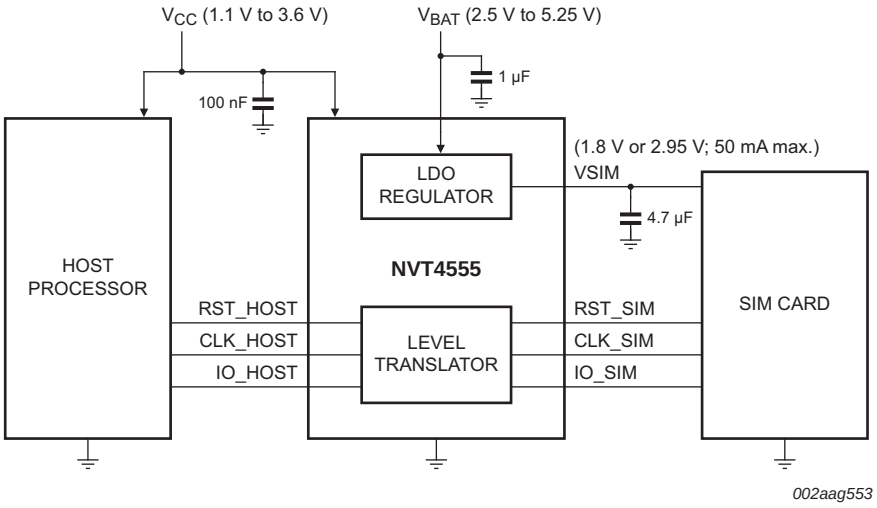


Fig 6. NVT4555 application circuit interfacing with typical SIM card

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10.1 Input/output capacitor considerations

It is recommended that a 1 μF and 100 nF capacitors having low Equivalent Series Resistance (ESR) are used respectively at the battery (V_{BAT}) and V_{CC} input terminals of the NVT4555. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

Also, a 4.7 μF capacitor is recommended at the Low Dropout regulator (LDO) output terminal to ensure stability. X5R and X7R type are recommended for their minimal variation over temperature and low ESR over frequency which avoids stability issues at high frequencies. The maximum ESR should be < 1.0 Ω. Furthermore, the decrease in capacitance with an increase in the bias voltage should be considered to optimize LDO stability. In addition, the trade-off in LDO stability versus the value and constraint in case size of the capacitor determined by the application must be considered. As output load capacitance decreases, the LDO stability becomes marginal. Given that a 4.7 μF ceramic capacitor may drop by 80 % in capacitance depending on the effects of bias voltage and temperature, it is recommended to refer to the manufacturer's characterization of a capacitor based on case size, bias voltage and type. Figure 7 is an example of how a 4.7 μF capacitor is affected by the above parameters.

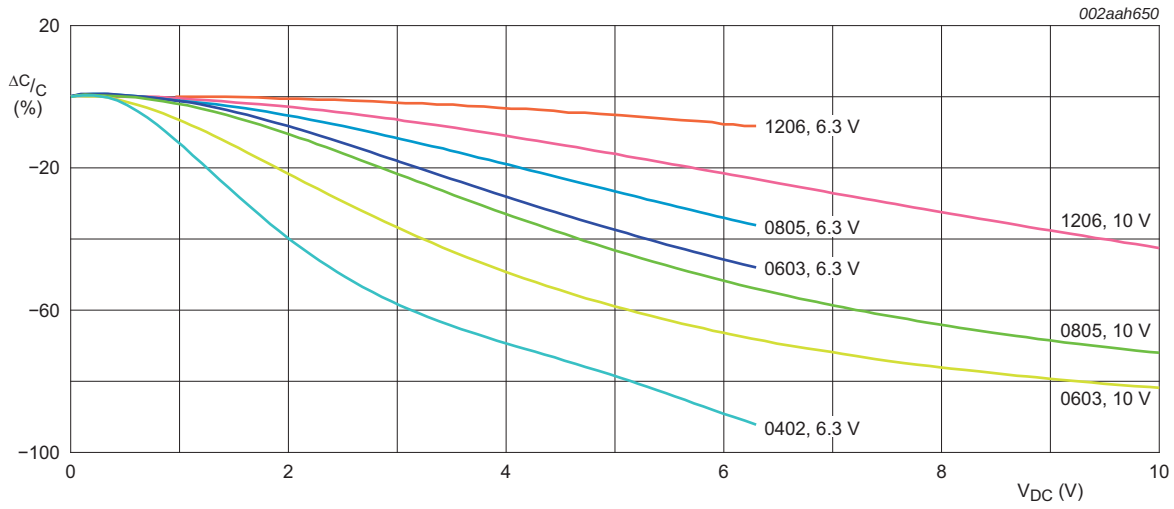

Fig 7. Variation of capacitance for a 4.7 μF capacitor versus DC voltage, value, case size and type

10.2 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. Since the internal band gap regulator is the dominant noise source in a typical application, connections and routing of the ground is very important to improve and optimize noise performance, PSRR and transient response. It is recommended to design the PCB so that the V_{CC}, V_{BAT} and VSIM pins are bypassed with a capacitor with each ground returning to a common node at the GND pin of the NVT4555 such that ground loops are minimized.

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10.3 Dropout voltage

The NVT4555 uses a PMOS pass transistor to achieve a very low dropout voltage. When $V_{BAT} - V_{O(reg)}$ (VSIM pin) is less than the dropout voltage, the PMOS transistor operates in the linear region and the input-to-output resistance is R_{DSon} of the PMOS device. The dropout voltage, V_{do}, will scale with the output current since the PMOS device behaves like a resistor in the input-to-output path.

10.4 Level translator stage

The architecture of the NVT4555 I/O channel is shown in Figure 8. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW.

The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

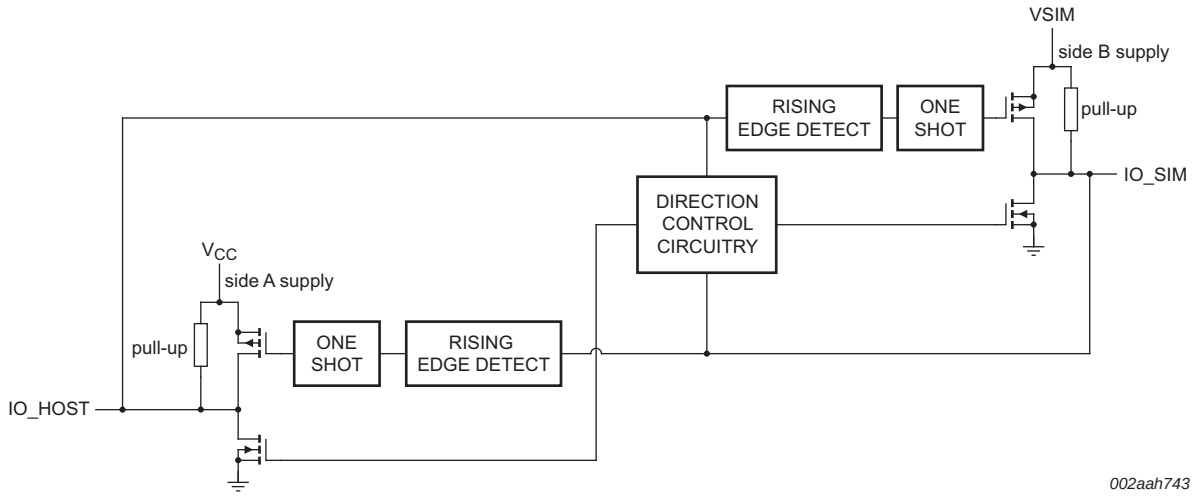

Fig 8. Automatic direction control level translator for HIGH-level direction change interfaces

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10.5 LDO block diagram

The LDO's block diagram is depicted in Figure 9. It contains a pull-down mechanism to avoid any uncontrolled voltage level at the VSIM pin in the disabled state. Furthermore, thermal protection as well as an overcurrent protection are integrated to disable the output in case of a permanent short that may result in excessive self-heating.

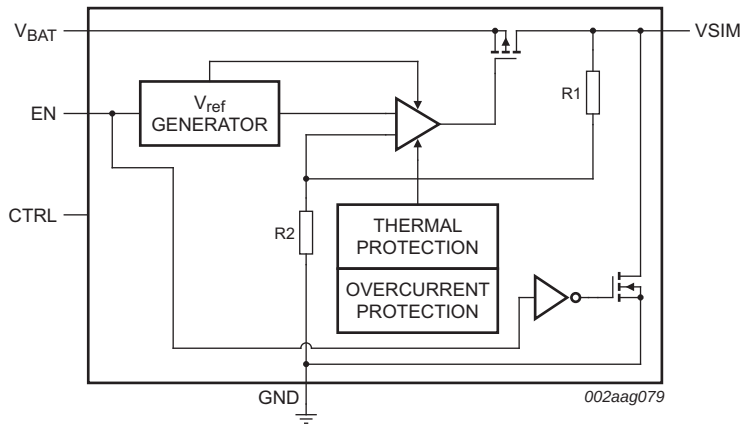

Fig 9. LDO block diagram

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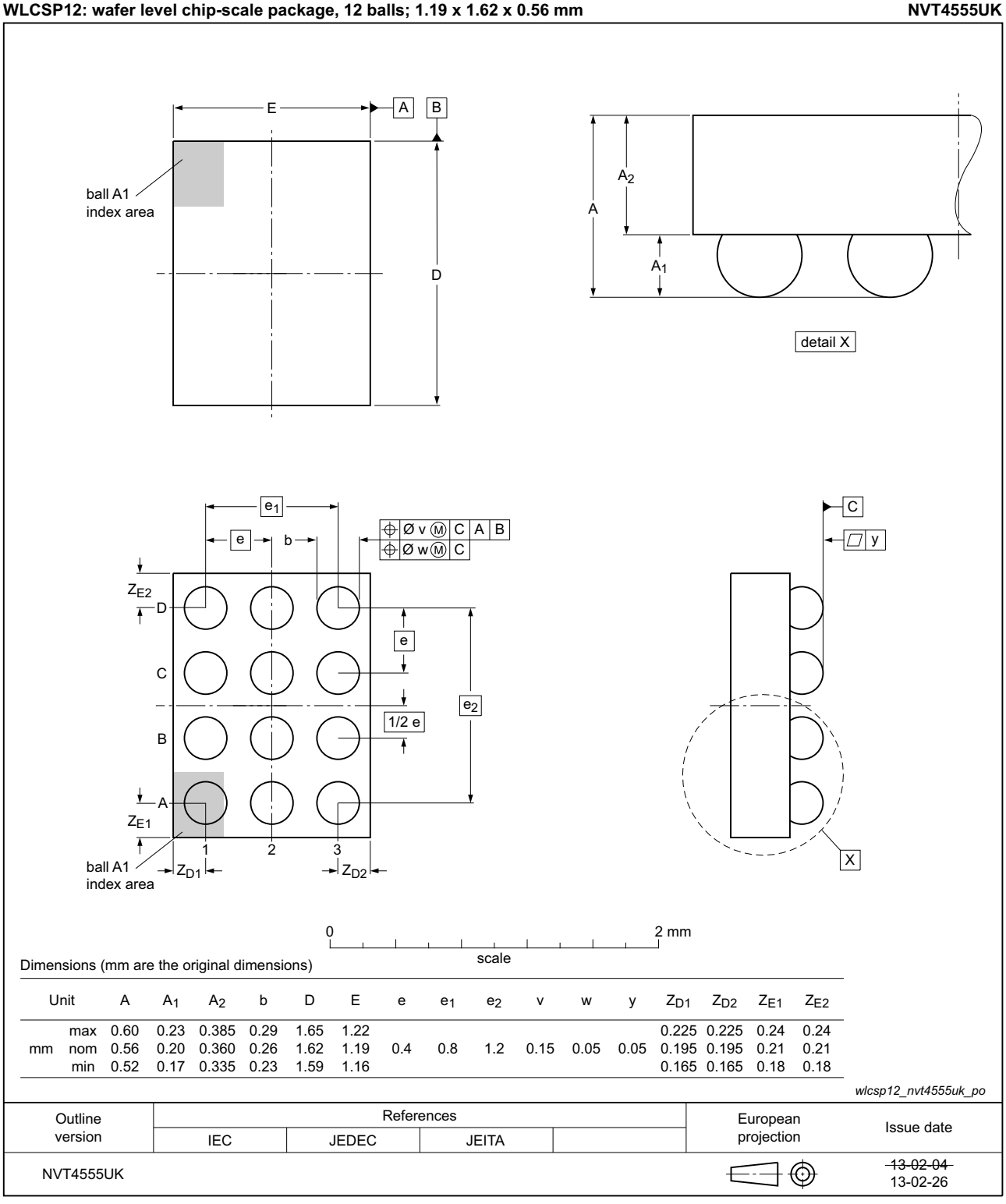
11. Package outline

WLCSP12: wafer level chip-scale package, 12 balls; 1.19 x 1.62 x 0.56 mm **NVT4555UK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}
	max	0.60	0.23	0.385	0.29	1.65	1.22							0.225	0.225	0.24	0.24
mm	nom	0.56	0.20	0.360	0.26	1.62	1.19	0.4	0.8	1.2	0.15	0.05	0.05	0.195	0.195	0.21	0.21
	min	0.52	0.17	0.335	0.23	1.59	1.16							0.165	0.165	0.18	0.18

wlcsp12_nvt4555uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NVT4555UK						~~13-02-04~~ 13-02-26

Fig 10. Package outline NVT4555UK (WLCSP12)

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12. Soldering of WLCSP packages

12.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

12.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

12.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9.

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.

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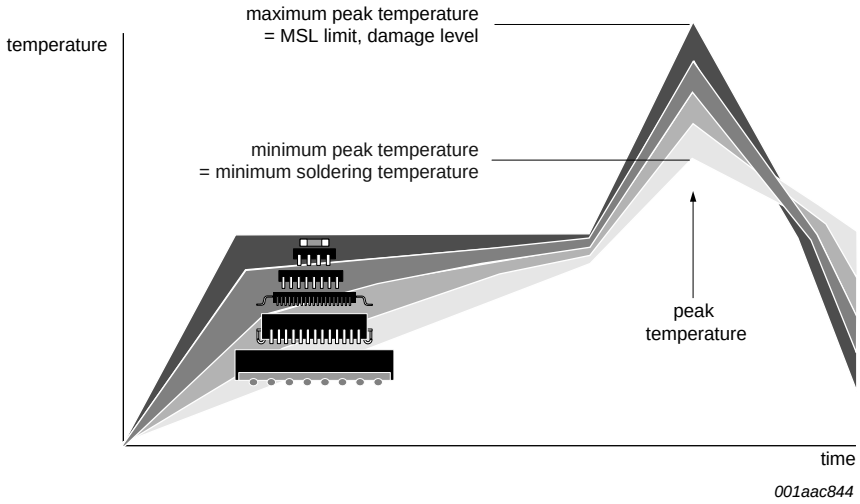

MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

12.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

12.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

12.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

12.3.4 Cleaning

Cleaning can be done after reflow soldering.

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DP	Dry Pack
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HBM	Human Body Model
I/O	Input/Output
LDO	Low DropOut regulator
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
SIM	Subscriber Identification Module

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4555 v.2	20130524	Product data sheet	-	NVT4555 v.1
Modifications:	• Table 3 "Pin description": – description for CTRL pin corrected from "VSIM = 3 V" to "VSIM = 2.95 V" – description for VSIM pin corrected from "3 V (CTRL = 1)" to "2.95 V (CTRL = 1)" – description for IO_HOST pin corrected from "open-drain configuration" to "open-drain driver" – deleted 4 "n.c." rows from table (correction) • Table 4 "Function selection": VSIM output voltage for selection "11" corrected from "3.0 V" to "2.95 V" • Figure 6 "NVT4555 application circuit interfacing with typical SIM card" supply voltage corrected from "V_{CC} (1.1 V to 3.0 V)" to "V_{CC} (1.1 V to 3.6 V)" • Figure 8 "Automatic direction control level translator for HIGH-level direction change interfaces": – corrected connection for 2 (P-type channel) transistors – corrected signal name from "IO_HOST/EN" to "IO_HOST"			
NVT4555 v.1	20130501	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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